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Full-Array Boolean Logic CIM Macro with Self-Recycling 10T-Sram Cell for AES Systems

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ABSTRACT: Static random access memory (SRAM) has become one of the most essential building blocks in modern low-power and high-speed digital systems such as portable electronics, signal processing units, and encryption engines. Conventional 6T and 8T SRAM cells provide compact design and fast access, but they suffer from limited noise margins, high leakage power, and additional circuit requirements for logical operations, leading to larger delay and power consumption. To address these issues, recent research explored 9T and 10T SRAM designs, which improve stability and reduce leakage but often lack efficient integration for logic-in-memory applications. In this work, we developed a single-bit 10T SRAM cell in 45 nm CMOS technology and extended it into an 8×8 SRAM array. The novelty of this design lies in combining stable storage with logic computation, where the SRAM array is not only used for memory but also performs in-built OR, XOR, and AND logic gate operations without requiring additional dedicated hardware. This approach directly improves energy efficiency and speed while minimizing the overhead of extra circuits. We evaluated the design under varying supply voltages, measuring delay and power consumption, and observed enhanced read–write stability, reduced dynamic power, and faster logic execution compared with conventional SRAM structures. The entire design was tested using industry-standard simulation platforms with 45 nm CMOS technology to ensure realistic validation. These results indicate that the proposed 10T SRAM-based memory-logic array offers strong potential for embedded computing systems where both storage and basic Boolean logic operations are needed within the same architecture, making it highly suitable for portable devices, medical electronics, and encryption accelerators.

KEYWORDS: Compute-In-Memory (CIM), 10T-SRAM, AES, Boolean Logic, Self-Recycling, Cryptographic Hardware, Low Power Design, Parallel Processing, Embedded Systems, Hardware Security.

I. INTRODUCTION

A digital system can be described at different levels of abstraction and from different points of view. An HDL should faithfully and accurately model and describe a circuit, whether already built or under development, from either the structural or behavioural views, at the desired level of abstraction. Because HDLs are modelled after hardware, their semantics and use are very different from those of traditional programming languages. There are several EDA (Electronic Design Automation) tools available for circuit synthesis, implementation, and simulation using VHDL. Some tools (place and route, for example) are ordered as part of a vendor's design suite (e.g., Altera's Quartus II, which allows the synthesis of VHDL code onto Altera's CPLD/FPGA chips, or Xilinx's ISE suite, for Xilinx's CPLD/FPGA chips). Other tools (synthesizers, for example), besides being ordered as part of the design suites, can also be provided by specialized EDA companies (Mentor Graphics, Synopsis, Simplicity, etc.). FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

II. LITRATURE SURVEY

Physical mechanisms responsible for nondestructive single-event effects in digital microelectronics are reviewed, [1] concentrating on silicon MOS devices and integrated circuits. A brief historical overview of single-event effects in space and terrestrial systems is given, and upset mechanisms in dynamic random access memories, static random access memories, and combinational logic are detailed. Techniques for mitigating single-event upset are described, as well as methods for predicting device and circuit single-event response using computer simulations. The impact of technology trends on single-event susceptibility and future areas of concern are explored. [2] addresses the problem of multiple-node upsets in nanoscale CMOS storage elements due to scaling. A novel 13T Schmitt Trigger-based memory cell is proposed to improve soft-error tolerance compared to the conventional 12T DICE cell. The 13T cell achieves better resilience under charge sharing and collection effects. [3] We propose a quad-node ten transistor (10 T) soft error robust SRAM cell that offers differential read operation for robust sensing. The cell exhibits larger noise margin in sub-0.45 V regime and 26% less leakage current than the traditional soft error tolerant 12 T DICE SRAM cell. When compared to a conventional 6 T SRAM cell, the proposed cell offers similar noise margin as the 6 T cell at half the supply voltage, thus significantly saving the leakage power. [4] In this paper, a novel low-power and highly reliable radiation hardened memory cell (RHM-12T) using 12 transistors is proposed to provide enough immunity against single event upset in TSMC 65 nm CMOS technology.

III. METHODOLOGY

The methodology for designing the **Full-Array Boolean Logic CIM Macro with Self-Recycling 10T-SRAM Cell for AES Systems** focuses on achieving high performance, low power consumption, and efficient in-memory computation. The implementation is carried out through the following structured phases:

1. Requirement Analysis and Problem Identification: The first step involves analyzing the limitations of conventional AES implementations in traditional architectures. Key challenges such as high latency, excessive data movement, increased power consumption, and limited parallelism are identified. The requirements for a high-speed, low-power, and secure computation model are defined, particularly for embedded and IoT applications.

2. Design of Compute-In-Memory (CIM) Architecture: A CIM-based architecture is developed where both storage and computation are integrated within the same memory array. The design enables in-memory execution of Boolean operations required for AES, reducing dependency on external processing units. The architecture supports row-wise and column-wise parallel operations across the memory array.

3. Development of 10T-SRAM Cell: A 10-Transistor SRAM cell is designed to improve stability and reliability during read/write operations. Unlike traditional 6T-SRAM cells, the 10T design separates read and write paths, minimizing read disturbance and improving noise margins. This ensures safe and accurate in-memory computation.

4. Implementation of Self-Recycling Mechanism: A self-recycling technique is incorporated into the SRAM design to reuse internal charge during switching operations. This reduces dynamic power consumption and improves overall energy efficiency. The mechanism helps in minimizing energy loss, especially during repetitive operations involved in AES processing.

5. Integration of Full-Array Boolean Logic Operations: Boolean logic functions such as AND, OR, XOR, and NOT are implemented directly within the SRAM array. Full-array activation enables simultaneous execution of these operations across multiple memory cells, achieving massive parallelism. This significantly accelerates computation compared to sequential processing methods.

6. Mapping of AES Algorithm to CIM Architecture: The AES encryption process is mapped onto the CIM framework. Core AES operations such as:

- SubBytes
- ShiftRows
- MixColumns
- AddRoundKey

are optimized using in-memory Boolean logic operations. This mapping ensures efficient execution of encryption and decryption processes within the memory array.

7. Circuit Simulation and Implementation : The designed architecture is simulated using hardware design and circuit simulation tools. Parameters such as voltage levels, switching behavior, delay, and power consumption are analyzed. The functionality of the 10T-SRAM cell and CIM operations is verified through simulation results.

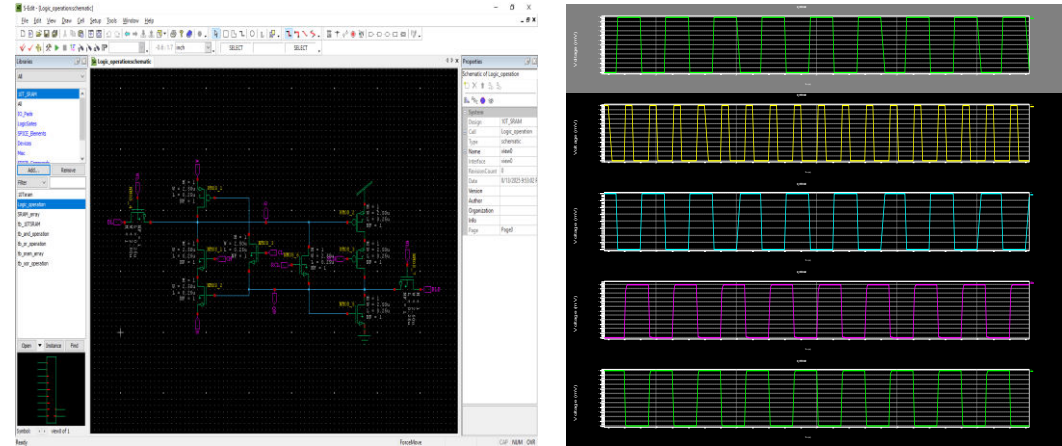


Fig. 4.1 Logic operation using 10T SRAM

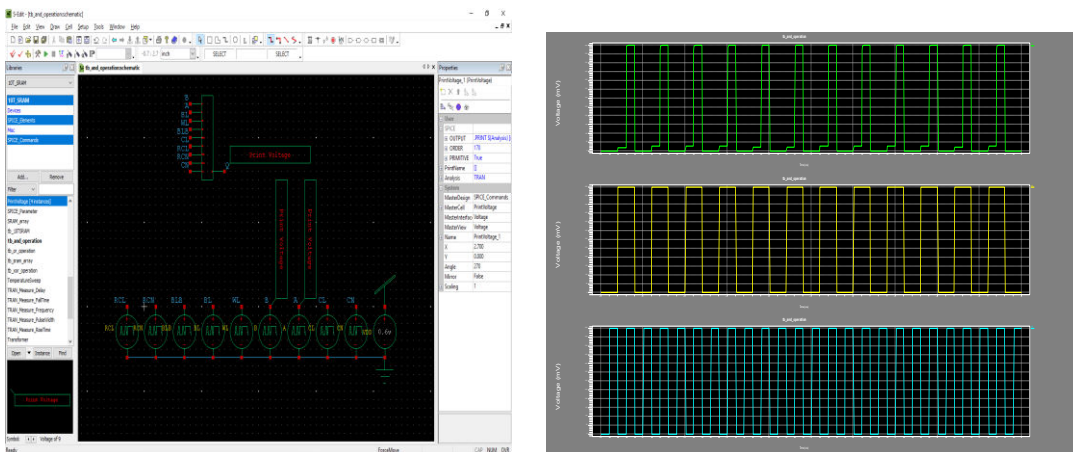


Fig. 4.2 AND Operation using 10T SRAM

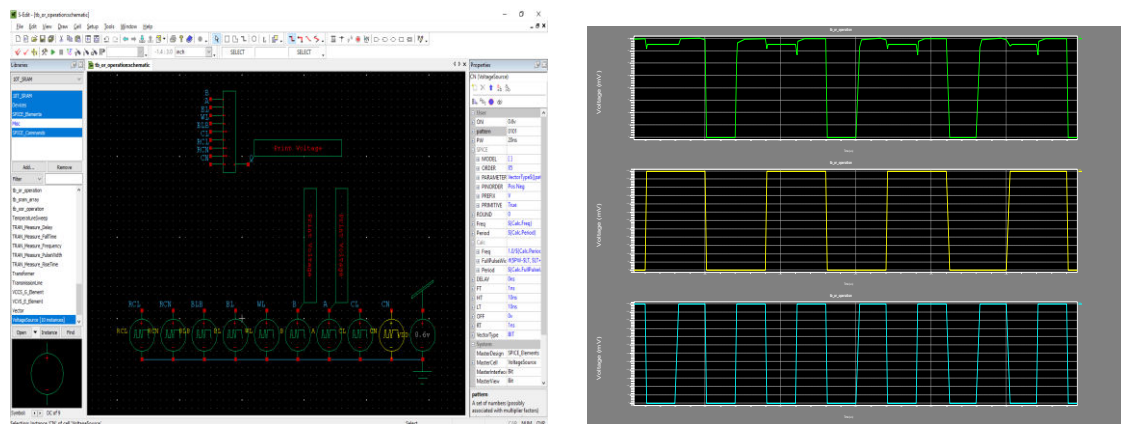


Fig. 4.3 OR operation using 10T SRAM

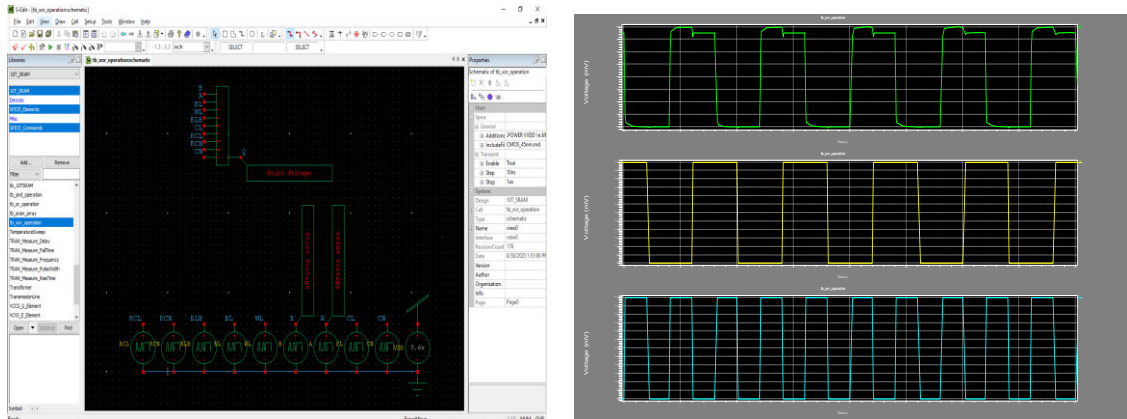


Fig. 4.4 XOR Operation using 10T SRAM

The 10T design minimizes read disturbance and improves noise margins, ensuring accurate data storage and computation. system minimizes energy loss and achieves higher energy efficiency. reduction in dynamic power consumption compared to conventional SRAM-based designs. In terms of performance metrics, the proposed CIM macro achieves:

- Reduced latency**, due to in-memory computation and elimination of unnecessary data transfer
- Higher throughput**, enabled by parallel full-array operations
- Lower power consumption**, due to self-recycling and optimized SRAM design
- Improved energy efficiency**, making it suitable for low-power applications.

V. CONCLUSION

In this work, a **Full-Array Boolean Logic Compute-In-Memory (CIM) Macro using a Self-Recycling 10T-SRAM Cell for AES Systems** has been successfully designed and analyzed to address the limitations of conventional computing architectures. The proposed system effectively overcomes the challenges associated with the **von Neumann bottleneck** by enabling computation directly within the memory array, thereby reducing data movement, latency, and energy consumption. The integration of **full-array Boolean logic operations** allows parallel execution of AES functions, significantly improving processing speed and throughput. The use of a **10T-SRAM cell** enhances stability, reduces read disturbance, and ensures reliable in-memory computation. Additionally, the incorporation of a **self-recycling mechanism** plays a crucial role in minimizing power consumption by reusing internal charge, making the system highly energy-efficient. Overall, the proposed CIM-based AES system provides a scalable, secure, and efficient solution for next-generation computing environments. It is particularly well-suited for applications such as IoT devices, embedded systems, and edge computing, where low power consumption and high performance are critical. This work highlights the potential of combining advanced memory design with in-memory computing techniques to develop high-performance cryptographic systems.

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